Unformatted Serial Link

Remote Digital Capture of Noisy Signals

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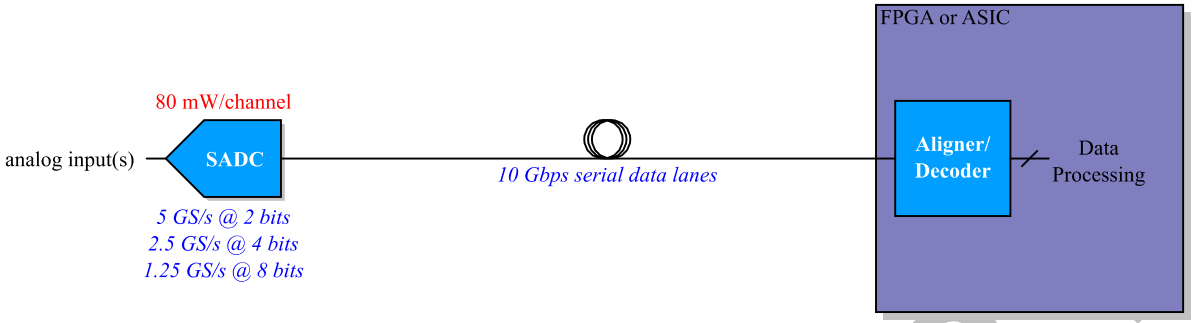

Applications

- Scientific and Medical Instrumentation
- Remote Sensing
- Radar/Sonar cameras (commercial or military)
- Imaging Scanners (medical, industrial, security)
- Aerospace and Astronomy Instrumentation
- Mobile Instrument Platforms (UAV, cube-sat)

Description

Based on a patented algorithm for reliable de-serialization of unformatted data streams, this sampler and decoder chipset enables high-throughput data transport with the minimum possible digital overhead and power dissipation at the source.

This complete end-to-end data collection and transport solution comprises two parts: An ultra-low-power, high-speed Serial-output Analog-to-Digital Converter (SADC) at the front-end, and a data re-alignment and decoding processor at the back-end. Together, these parts create a fully-functional data link capable of streaming raw samples at up to 5 Giga-samples per second from a front-end analog sensor. To work, the input signal needs only to meet certain minimum statistical requirements that are typical of almost any naturally-occurring or noise-laden analog waveform.

The front-end SADC has been optimized to achieve high data-rates with the minimum possible pin-count, power dissipation, and digital emissions which could otherwise interfere with sensitive front-end analog electronics. Available as a dual-channel ADC, it consumes only 80 mW/channel, while supporting dynamically-variable bit resolution from 2- to 8-bits with inversely proportional sample rates for a total data throughput of 10 Gbps per lane. Each input channel is digitized and delivered to CML-compatible outputs capable of driving industry-standard small-form-factor pluggable fiber-optic transceivers (e.g. SFP, SFP+, and QSFP). Alternatively, both channels may be interleaved onto a single CML output for transmission of both data streams on a single lane at half the rate.

The aligner-decoder at the back-end of the link automatically detects the most-significant bits (MSBs) in the data stream, and identifies the samples coming from the two input channels (if they were interleaved at the front-end), presenting simultaneous samples at the output in parallel form as if the ADC was connected locally, making the serial-link and the associated physical separation effectively transparent to the back-end processor. The decoding algorithm is available as a Verilog building block that can be instantiated onto a user's custom ASIC or downloaded into an FPGA.

Features

- SADC Hard-Macro for UMC 40 nm CMOS
- Aligner/Decoder Verilog Code
- High data rate and versatile bit resolution
  - *5 GS/s @ 2 bits per lane*
  - *2.5 GS/s @ 4 bits per lane*
  - *1.25 GS/s @ 8 bits per lane*
- Dual-channel interleave mode
- Ultra-low front-end power: 80 mW/channel
- Ultra-small front-end footprint: <24 pins

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